IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Michael B. Galles, et al.
Serial No.:	10/696,146
Filing Date:	October 29, 2003
Confirmation No.:	5506
Group Art Unit:	2181
Examiner:	William M. Treat
Title:	MULTI-PURPOSE PROCESSOR SYSTEM AND METHOD OF ACCESSING DATA THEREIN

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

APPEAL BRIEF

Applicant has appealed to the Board of Patent Appeals and Interferences from the decision of the Examiner mailed May 12, 2010 rejecting Claims 1-20. Applicant respectfully submits herewith their brief on appeal.

REAL PARTY IN INTEREST

The present Application was assigned by the inventors to Silicon Graphics, Inc., a Delaware corporation, as indicated by an assignment from the inventors for the parent application recorded on October 15, 1999 in the Assignment Records of the United States Patent and Trademark Office at Reel 010325, Frames 0832-0836. Silicon Graphics, Inc. assigned a security interest in the Application to Wells Fargo Foothill Capital, Inc., as evidence by a document recorded on August 19, 2005 in the Assignment Records of the United States Patent and Trademark Office at Reel 016871, Frames 0809-0840. Silicon Graphics, Inc. also assigned a security interest in the Application to General Electric Capital Corporation, as evidence by a document recorded on August 24, 2006 in the Assignment Records of the United States Patent and Trademark Office at Reel 018545, Frames 0777-0841. General Electric Capital Corporation assigned its security interest in the Application to Morgan Stanley & Co., Incorporated, as evidence by a document recorded on October 18, 2007 in the Assignment Records of the United States Patent and Trademark Office at Reel 019995, Frames 0895-0960.

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal.

STATUS OF CLAIMS

Claims 1-20 stand rejected pursuant to an Official Action issued May 12, 2010. Claims 1-20 are all presented for appeal.

STATUS OF AMENDMENTS

Subsequent to the Official Action issued in the above identified Application from which appeal has been taken, no additional amendments to the claims have been made.

SUMMARY OF CLAIMED SUBJECT MATTER

With respect to Independent Claim 1, a multi-processor system 10 is provided. (See FIGURE 1 and page 7, lines 2-3). The multiprocessor system 10 includes a plurality of processors 12. (See FIGURE 1 and page 7, lines 3-4). Each processor 12 includes an integrated memory 16 operable to provide/receive/store data. (See FIGURE 1 and page 7, lines 5-8). Each processor includes a central processing unit 20 having an integrated memory controller 30 operable to control access to the integrated memory 16 and an integrated memory directory 18 operable to maintain a plurality of memory references to data within the integrated memory 16. (See FIGUREs 1 and 2 and page 8, lines 24-27, as amended May 23, 2006 and shown in the Evidence Appendix). The multiprocessor system 10 includes an external switch 14 coupled to each of the plurality of processors 12. (See FIGURE 1 and page 7, lines 3-10). The external switch 14 is operable to pass data to and from any of the plurality of processors 12. (See FIGURE 1 and page 7, lines 8-10). The external switch 14 includes an external directory 22. (See FIGURE 1 and page 7, lines 7-8). The external directory 22 is operable to provide a memory reference for each of the plurality of processors 12 to remote data that is not provided within its own integrated memory directory 18. (See FIGURE 1 and page 7, line 28, to page 8, line 5).

With respect to Independent Claim 11, a method of accessing data in a multi-processor system 10 is provided. The method includes storing information in a local memory 16 where the local memory is integrated within a particular one of a plurality of processors 12 of the multi-processor system 10. (See page 7, lines 5-7). A list of memory references to the information in the local memory 16 is maintained in a

memory directory 18 integrated with a central processing unit 20 of the particular one of the plurality of processors 12. (See FIGUREs 1 and 2; page 7, lines 5-7 and 14-16; and page 8, lines 24-27, as amended May 23, 2006 and shown in the Evidence Appendix). A request for data is generated. (See page 7, lines 28, to page 8, line 2). A determination is made as to whether the data is associated with information stored in the local memory 16 and has a memory reference in the memory directory 18. (See page 7, lines 28-31). The request is forwarded to an external switch 14 in response to the data not having a memory reference in the memory directory 18. (See page 7, line 28, to page 8, line 1). Data not having a memory reference to the local memory 16 in the memory directory 18 is stored in a remote memory 16. (See page 7, lines 28-31). A memory reference for the data is identified in response to the request. (See page 8, lines 3-5). The data from the remote memory 16 is obtained via the external switch 14 in response to the identified memory reference. (See page 8, lines 3-5).

With respect to Independent Claim 16, a processor 12 in a multi-processor system 10 is provided. (See FIGURE 1 and page 7, lines 2-3). The processor 12 includes a local memory 16 integrated in the processor 12 and operable to provide/receive/store data. (See FIGURE 1 and page 7, lines 5-7). The processor 12 includes a central processing unit 20. (See FIGUREs 1 and 2 and page 7, lines 5-7). A memory controller 30 is integrated in the central processing unit 20 and operable to control access to and from the local memory 16. (See FIGUREs 1 and 2 and page 8, lines 24-32, as amended May 23, 2006 and shown in the Evidence Appendix). A memory directory 18 is integrated in the central processing unit 20 and operable to maintain memory references to data within the local memory 16. (See FIGUREs 1 and 2 and page 7, lines 5-7

and 14-16). The memory directory 18 is operable to generate a data request for data not having a memory reference in the memory directory 18. (See Page 7, line 28, to page 8, line 1). The processor 12 includes a network interface 32 integrated in the processor 12 and operable to provide the data request to an external directory 22 external to the processor 12. (See FIGURE 2 and page 8, lines 27-29). The network interface 32 is operable to receive the data according to the data request. (See FIGURE 2 and page 8, lines 27-29).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-10 and 16-20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

2. Claims 1-20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

3. Claims 1-10 and 16-20 stand rejected under 35 U.S.C. §112, first paragraph, for containing subject matter not described in the specification.

4. Amendments made to the specification stand objected to under 35 U.S.C. §132(a) as introducing new matter.

5. The drawings stand objected under 37 C.F.R. §1.84(p)(5) for the inconsistencies between the specification and the drawings.

6. Claims 11-15 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,890,217 issued to Kabemoto, et al.

7. Claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,374,331 issued to Janakiraman, et al.

8. Claims 2, 3, 18, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,374,331 issued to Janakiraman, et al. in view of the Gupta paper.

ARGUMENT

1. Claims 1-10 and 16-20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

Independent Claims 1 and 16 provide the feature of a processor 12 with an integrated local memory 16. The processor also includes a central processing unit 20. See FIGURE 1. The central processing unit 20 includes a memory controller 30 integrated therein for controlling access to the local memory 16 and includes a memory directory 18 integrated therein that maintains a plurality of memory references to data in the local memory 16. See FIGURE 2. Thus, there is support in Applicant's specification for the terms of the claims. FIGURE 2 clearly shows a detailed view of processor 12, namely its central processing unit 20. Discrepancies between the drawings and the specification with respect to the claims were identified by the Examiner. To address inconsistencies between the drawings and the specification, minor amendments were made to the specification as requested by the Examiner. See the attached Evidence Appendix where a copy of a page from the Request for Continued Examination of May 23, 2006 showing the minor changes to the specification in order to provide consistency with the drawings as requested by the Examiner in the Final Action of February 23, 2006 are provided. Also attached therein is a copy of the original drawings of which no amendments have been made. However, no amendment to the specification was needed as FIGURE 2 clearly supports the language provided in the claimed invention. The amendment to Applicant's specification was made to merely provide identification of FIGURE 2 as it is clearly depicted and provide consistency between Applicant's specification and the drawings to address an inconsistency identified and raised by the Examiner. As the central processing unit 20 is part of

processor 12, the use of the term 'processor 12' merely provides a global reference with respect to the operation of its internal components, the local memory and the central processing unit. Thus, no amendments were made to change the other instances of the term 'processor 12' in Applicant's specification. An amendment was only made to properly identify what FIGURE 2 clearly depicts. Moreover, one of skill in the art would readily realize and reconcile FIGUREs 1 and 2 with Applicant's specification based on what is depicted therein. In addition, the Examiner readily admits one can provide support that FIGURE 2 depicts the central processing unit 20. FIGURE 2 is an original drawing figure that supports a central processing unit 20 having a memory controller 30 and a memory directory 18 as clearly depicted therein. Therefore, Applicant respectfully submits that there is full support for the claims in the Application.

2. Claims 1-20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

FIGURE 2 and Applicant's specification provide ample support for the claimed invention. FIGURE 2 clearly shows a central processing unit 20 having a memory controller 30 and a memory directory 18 integrated therein and, along with memory 16, being integrated into the single device of processor 12 shown in FIGURE 1. Moreover, the term 'integrated' is clearly defined in the specification as being within a single device. See page 7, lines 5-7, of Applicant's specification. FIGURE 2 shows that the memory controller 30 and the memory directory 18 are part of the central processing unit 20. Thus, there is ample support in Applicant's specification for the use of the term 'integrated' within the claims. Moreover, the Examiner readily admits that integration of the memory directory 18 in the central processing unit 20 is provided in the Application. Dependent Claims 2-10, 12-15, and 17-20 respectively depend from Independent Claims 1, 11, and 16 and are also in accordance with 35 U.S.C. §112, second paragraph, for the reasons specified above. Therefore, Applicant respectfully submits that Claims 1-20 are in compliance with 35 U.S.C. §112, second paragraph.

3. Claims 1-10 and 16-20 stand rejected under 35 U.S.C. §112, first paragraph, for containing subject matter not described in the specification.

For the written description requirement, the specification must reasonably convey to those skilled in the art that applicant was in possession of the claimed invention as of the date of the invention. M.P.E.P. §2106(V)(B).

The claimed invention subject matter need not be described literally, i.e., using the same terms, in order for the disclosure to satisfy the description requirement. M.P.E.P. §2106(V)(B). Support for the central processing unit having an integrated memory controller as required in Independent Claims 1 and 16 is clearly provided in FIGURE 2. FIGURE 2 is a detailed view of central processing unit 20. This is supported by the fact that the element is labeled with reference numeral 20 and includes directory 18 consistent with what is shown in FIGURE 1. Moreover, a link to memory 16, and not memory 16 itself, is shown in FIGURE 2 providing further basis that FIGURE 2 is a detailed view of CPU 20 within processor 12. Accordingly, memory controller 30 and memory directory 18 are clearly shown to be within central processing unit 20. Applicant's specification at page 7, lines 5-7, particularly discloses that these components are integrated with memory 16 into a single device, processor 12. Thus, the specification provides clear support for the claim language. Dependent Claims 2-10 and 17-20 respectively depend from Independent Claims 1 and 16 and also satisfy the written description requirement for the reasons specified above. Therefore, Applicant respectfully submits that Claims 1-10 and 16-20 are in compliance with 35 U.S.C. §112, first paragraph.

4. Amendments made to the specification stand objected to under 35 U.S.C. §132(a) as introducing new matter.

Applicant respectfully submits that no new matter has been added into the specification. Changes to the specification have been made to provide consistency with what is clearly shown in FIGURE 2 and requested by the Examiner. Attached herewith in the Evidence Appendix is a copy of a page from the Request for Continued Examination of May 23, 2006 showing the minor changes to the specification in order to provide consistency with the drawings as requested by the Examiner in the Final Action of February 23, 2006. Also attached herewith is a copy of the original drawings of which no amendments have been made. FIGURE 2 clearly illustrates the make up of central processing unit 20 of processor 12. The element is labeled 20 as similarly provided in FIGURE 1. Memory directory 18 is consistently shown to be within element 20, the central processing unit, in both FIGUREs 1 and 2. Furthermore, the absence of memory 16 from FIGURE 2 is further consistent with FIGURE 2 being only a depiction of central processing unit 20. Thus, changes to the specification have been appropriately made based on what is shown in FIGURE 2 without adding any new matter.

The Examiner relies on a the fact that reference numeral 18 in FIGURE 2 could be seen as a typo and should be a 12. However, this makes no sense as reference numeral 18 correctly identifies the memory directory within central processing unit 20 and could not be mistaken to be representing processor 12. The '7 mentions of processor 12' are merely global referrals to the operations being performed, namely by memory controller 30 and memory directory 18 within central processing unit 20 of processor 12. Moreover, the scope of the claims of the parent application are not changed as all elements are a part

of an overall processor 12 which is still consistently provided herein. Therefore, Applicant respectfully submits that the changes made to the specification are in accordance with 35 U.S.C. §132(a).

5. The drawings stand objected under 37 C.F.R. §1.84(p)(5) for including reference signs not mentioned in the specification.

As fully discussed above, minor amendments to Applicant's specification have already been made to address the inconsistency identified by the Examiner by properly identifying what is clearly depicted in FIGURE 2 as requested by the Examiner. Therefore, Applicant respectfully submits that the drawings are in accordance with 37 C.F.R. §1.84(p)(5).

6. Claims 11-15 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,890,217 issued to Kabemoto, et al.

Independent Claims

To anticipate a claim under 35 U.S.C. §102(e), a single prior art reference must teach each and every limitation as set forth in the claims. Since the cited prior art reference does not teach each and every element set forth in the claims, Applicant respectfully traverses this rejection.

Independent Claim 11 recites ". . . storing information in a local memory, the local memory being integrated within a particular one of a plurality of processors of the multi-processor system; maintaining a list of memory references to the information in the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors . . ."

By contrast, the Kabemoto, et al. patent shows processor and cache units separate from each other and a separate memory control module. Moreover, local memory 28 of the Kabemoto, et al. patent is shown to be associated with, but separate and apart from, its four processor elements 14-1 to 14-4 in FIG. 3. Thus, the Kabemoto, et al. patent fails to disclose storing information in a local memory integrated within a particular one of a plurality of processors as required by the claimed invention. Further, a directory memory 30 is disclosed as being associated with, but separate and apart from, four processor elements 14-1 to 14-4 and their respective CPUs 34 in FIG. 3 of the Kabemoto, et al. patent. As a result, the processor elements and associated CPUs of the Kabemoto, et al. patent do not include the feature of a memory directory integrated with a central processing unit of a

particular processor for maintaining a list of memory references to the information in the local memory within the particular processor as required by Independent Claim 11. Therefore, Applicant respectfully submits that Independent Claim 11 is not anticipated by the Kabemoto, et al. patent.

Dependent Claims

Dependent Claims 12-15 depend from Independent Claim 11 and are patentably distinct from the Kabemoto, et al. patent for the reasons discussed above. Therefore, Applicant respectfully submits that Dependent Claims 12-15 are not anticipated by the Kabemoto, et al. patent.

7. Claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,374,331 issued to Janakiraman, et al.

Independent Claims

Independent Claim 1 recites ". . . each processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory . . ." Similarly, Independent Claim 16 recites ". . . a local memory integrated in the processor and operable to provide/receive/store data; a central processing unit; a memory controller integrated in the central processing unit and operable to control access to and from the local memory; a memory directory integrated in the central processing unit and operable to maintain memory references to data within the local memory, the memory directory operable to generate a data request for data not having a memory reference in the memory directory . . ." Independent Claim 11 recites ". . . storing information in a local memory, the local memory being integrated within a particular one of a plurality of processors of the multi-processor system; maintaining a list of memory references to the information in the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors . . ."

By contrast, the Janakiraman, et al. patent shows a memory controller 2520 separate from its processor 2540. Thus, the Janakiraman, et al. patent fails to disclose a memory controller integrated in the central processing unit

and operable to control access to and from the local memory as required in Independent Claims 1 and 16. Further, the Janakiraman, et al. patent shows a coherency directory 6030 separate and apart from any of its processors 2540 and 3540. The Janakiraman, et al. patent also shows a directory cache being associated with two processors 2040 and 2050. Thus, the Janakiraman, et al. application fails to disclose a memory directory integrated with a central processing unit of a particular processor as required by Independent Claims 1, 11, and 16. The Examiner argues that it would be obvious to one of skill in the art from the Janakiraman, et al. patent to bring the directory cache on-chip. However, other than the Examiner's unsupported conclusory justification, there is no evidence of record from the prior art to support the leap the Examiner is making to justify the rejection of the claims on this point. Moreover, the Janakiraman, et al. patent teaches away from placing coherence control on the processor chip. The Janakiraman, et al. patent clearly states that it is not desirable to locate the coherence control on the processor chip collocated with the memory controller. See col. 8, lines 29-35, of the Janakiraman, et al. patent. Even assuming that one of skill in the art would make such a leap to bring a directory cache on chip, there is still no disclosure in the Janakiraman, et al. patent for having a memory directory in a central processing unit of a processor as required by the claimed invention. Therefore, Applicant respectfully submits that Claims 1, 11, and 16 are patentably distinct from the Janakiraman, et al. patent.

Dependent Claims

Dependent Claims 2-10, 12-15, and 17-20 depend from Independent Claims 1, 11, and 20 and are patentably distinct

from the Janakiraman, et al. patent for the reasons discussed above. Therefore, Applicant respectfully submits that Dependent Claims 2-10, 12-15, and 17-20 are not anticipated by the Janakiraman, et al. patent.

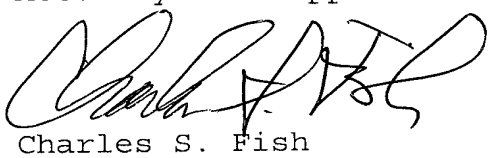
8. Claims 2, 3, 18, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,374,331 issued to Janakiraman, et al. in view of the Gupta paper. Independent Claim 1, from which Claims 2 and 3 depend, and Independent Claim 16, from which Claims 18 and 20 depend, have been shown above to be patentably distinct from the Janakiraman, et al. patent. Therefore, Applicant respectfully submits that Claims 2, 3, 18, and 20 are patentably distinct from the Janakiraman, et al. patent.

CONCLUSION

Applicant has clearly demonstrated that the present invention as claimed is clearly distinguishable over all the art cited of record, either alone or in combination, and satisfies all requirements under 35 U.S.C. §§101, 102, and 103, and 112. Therefore, Applicant respectfully requests the Board of Patent Appeals and Interferences to reverse the final rejection of the Examiner and instruct the Examiner to issue a Notice of Allowance of all claims.

The Commissioner is hereby authorized to charge any fees or credit any overpayments associated with this Application to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P.

Respectfully submitted,
BAKER BOTTS L.L.P.
Attorneys for Applicant



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12 January 2011

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CLAIMS APPENDIX

1. (Previously Presented) A multi-processor system, comprising:

a plurality of processors, each processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit having an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory and at least one memory reference to data within an integrated memory of a different processor;

an external switch coupled to each of the plurality of processors, the external switch operable to pass data to and from any of the plurality of processors, the external switch including an external directory, the external directory operable to provide a memory reference for each of the plurality of processors to remote data that is not provided within its own integrated memory directory.

2. (Original) The multi-processor of Claim 1, wherein the integrated memory directory is a cache buffer operable to hold a plurality of most recently accessed memory references.

3. (Original) The multi-processor system of Claim 2, wherein the integrated memory directory is operable to overwrite an oldest memory reference with a new memory reference upon reaching a buffer limit.

4. (Previously Presented) The multi-processor of Claim 1, wherein the integrated memory directory of a particular processor is operable to generate a directory request in response to not having a memory reference to data desired by its associated processor.

5. (Original) The multi-processor system of Claim 1, wherein the external directory is operable to receive a request for directory assistance from a particular one of the plurality of processors, the directory assistance request including a request for data not having a memory reference in the integrated memory directory of the particular one of the plurality of processors.

6. (Original) The multi-processor system of Claim 5, wherein the external directory is operable to generate a memory reference for the requested data.

7. (Original) The multi-processor device of Claim 5, wherein the external switch is operable to provide the generated memory reference to the integrated memory directory of the particular one of the plurality of processors in accordance with the request for data.

8. (Original) The multi-processor system of Claim 5, wherein the external switch is operable to provide the requested data to the particular one of the processors in response to the generated memory reference.

9. (Original) The multi-processor of Claim 1, wherein each of the plurality of processors includes an integrated network interface operable to communicate information to and from the external switch.

10. (Original) The multi-processor system of Claim 1, wherein the memory references in the external directory are represented in a same manner as memory references in a particular integrated memory directory.

11. (Previously Presented) A method of accessing data in a multi-processor system, comprising:

storing information in a local memory, the local memory being integrated within a particular one of a plurality of processors of the multi-processor system;

maintaining a list of memory references to the information in the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors;

maintaining at least one memory reference to information in the local memory of a different one of the plurality of processors in the memory directory integrated with the central processing unit of the particular one of the plurality of processors;

generating a request for data;

determining whether the data is associated with information stored in the local memory and has a memory reference in the memory directory;

forwarding the request to an external switch in response to the data not having a memory reference in the memory directory, wherein the data not having a memory reference to the local memory in the memory directory is stored in a remote memory;

identifying a memory reference for the data in response to the request;

obtaining the data from the remote memory via the external switch in response to the identified memory reference.

12. (Original) The method of Claim 11, further comprising:

obtaining the memory reference to the data stored in the remote memory.

13. (Original) The method of Claim 11, wherein the local memory is integrated with a particular one of a plurality of processors of the multi-processor system, the list of memory references being maintained in a memory directory integrated with the local memory in the particular one of the plurality of processors.

14. (Original) The method of Claim 13, wherein the identified memory reference is generated external to the particular one of the plurality of processors.

15. (Previously Presented) The method of Claim 13, further comprising:

obtaining the data in response to the memory directory maintaining a memory reference to the data.

16. (Previously Presented) A processor in a multi-processor system, comprising:

a local memory integrated in the processor and operable to provide/receive/store data;

a central processing unit;

a memory controller integrated in the central processing unit and operable to control access to and from the local memory;

a memory directory integrated in the central processing unit and operable to maintain memory references to data within the local memory, the memory directory operable to maintain at least one memory reference to data within a local memory integrated in a different processor, the memory directory operable to generate a data request for data not having a memory reference in the memory directory;

a network interface integrated in the processor and operable to provide the data request to an external directory external to the processor, the network interface operable to receive the data according to the data request.

17. (Original) The processor of Claim 16, wherein the memory directory maintains a list of most recently accessed memory references.

18. (Original) The processor of Claim 16, wherein the local memory has a capacity of four gigabytes of data and the memory directory has a capacity of eight megabytes of data memory reference.

19. (Original) The processor of Claim 16, wherein the network interface is operable to provide a memory reference generated by the external directory to the memory directory.

20. (Original) The processor of Claim 16, wherein the memory directory includes two to the power of eighteen memory references.

EVIDENCE APPENDIX

Attached herewith is a copy of page 2 from the Request for Continued Examination of May 23, 2006 showing changes to the specification to provide consistency with the drawing figures as requested by the Examiner.

Also attached herewith for reference purposes is a copy of a drawing sheet as originally filed showing FIGUREs 1 and 2.

IN THE SPECIFICATION

Please replace the paragraph at page 8, line 24, beginning with "FIGURE 2 is a block diagram . . . " as follows:

FIGURE 2 is a block diagram ~~of a~~ of central processing unit 20 of processor 12. Central processing unit 20 of processor ~~Processor~~ 12 includes ~~memory 16,~~ a memory controller 30 to interface with memory 16, memory directory 18, one or more network interfaces 32, and a CPU controller 34. Network interfaces 32 provide a communication capability between processor 12 and external switch 22. Memory controller 30 controls the read and write access from and to memory 16. CPU controller 34 controls flow between one or more processing units.

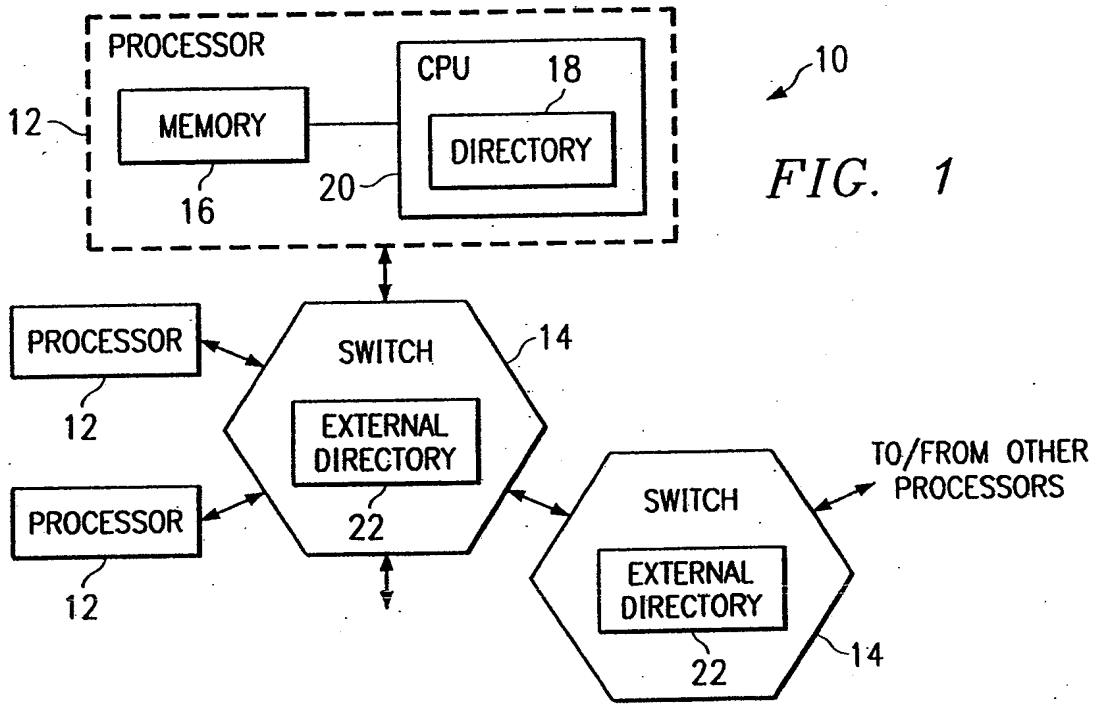
PROCESSOR
CPU
18
10
12
MEMORY
DIRECTORY
16
20
PROCESSOR
SWITCH
14
12
EXTERNAL
DIRECTORY
TO/FROM OTHER
PROCESSORS
PROCESSOR
22
SWITCH
12
EXTERNAL
DIRECTORY
14
22

FIG. 1

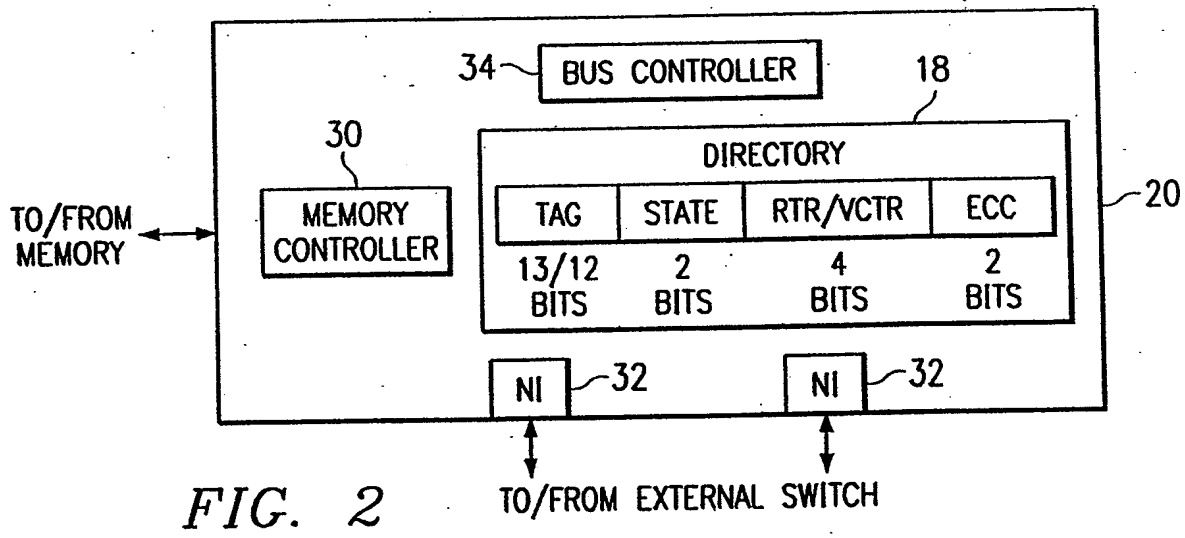
34
BUS CONTROLLER
18
30
DIRECTORY
TO/FROM
MEMORY
MEMORY
CONTROLLER
TAG
STATE
RTR/VCTR
ECC
20
13/12
BITS
2
BITS
4
BITS
2
BITS
NI
32
NI
32
TO/FROM EXTERNAL SWITCH

FIG. 2

RELATED PROCEEDINGS APPENDIX

None

CERTIFICATE OF SERVICE

None